Figure 1

Different hint extension instructions.

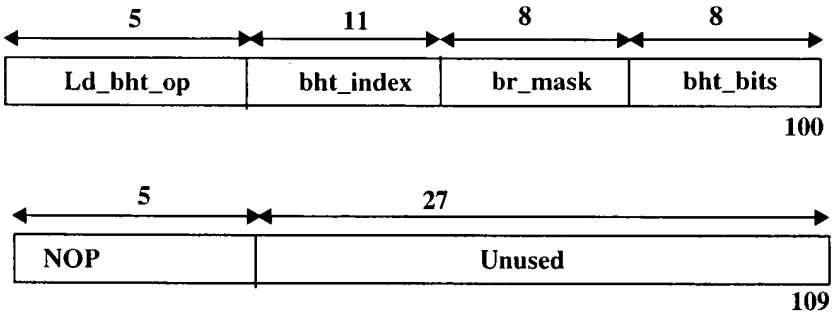


Figure 2

Overview of the Processor operation with Hint processor

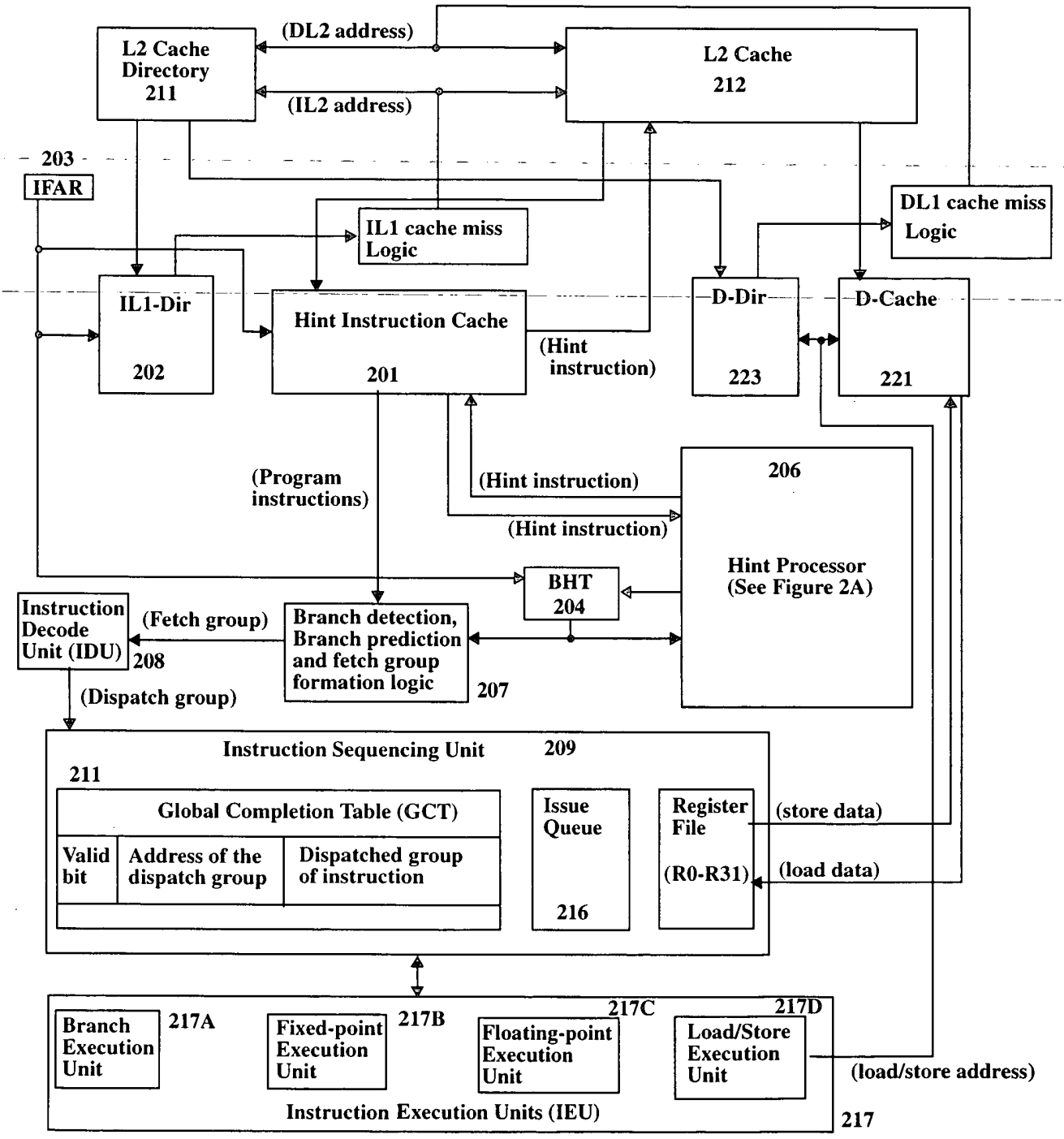


Figure 2A The Hint Processor

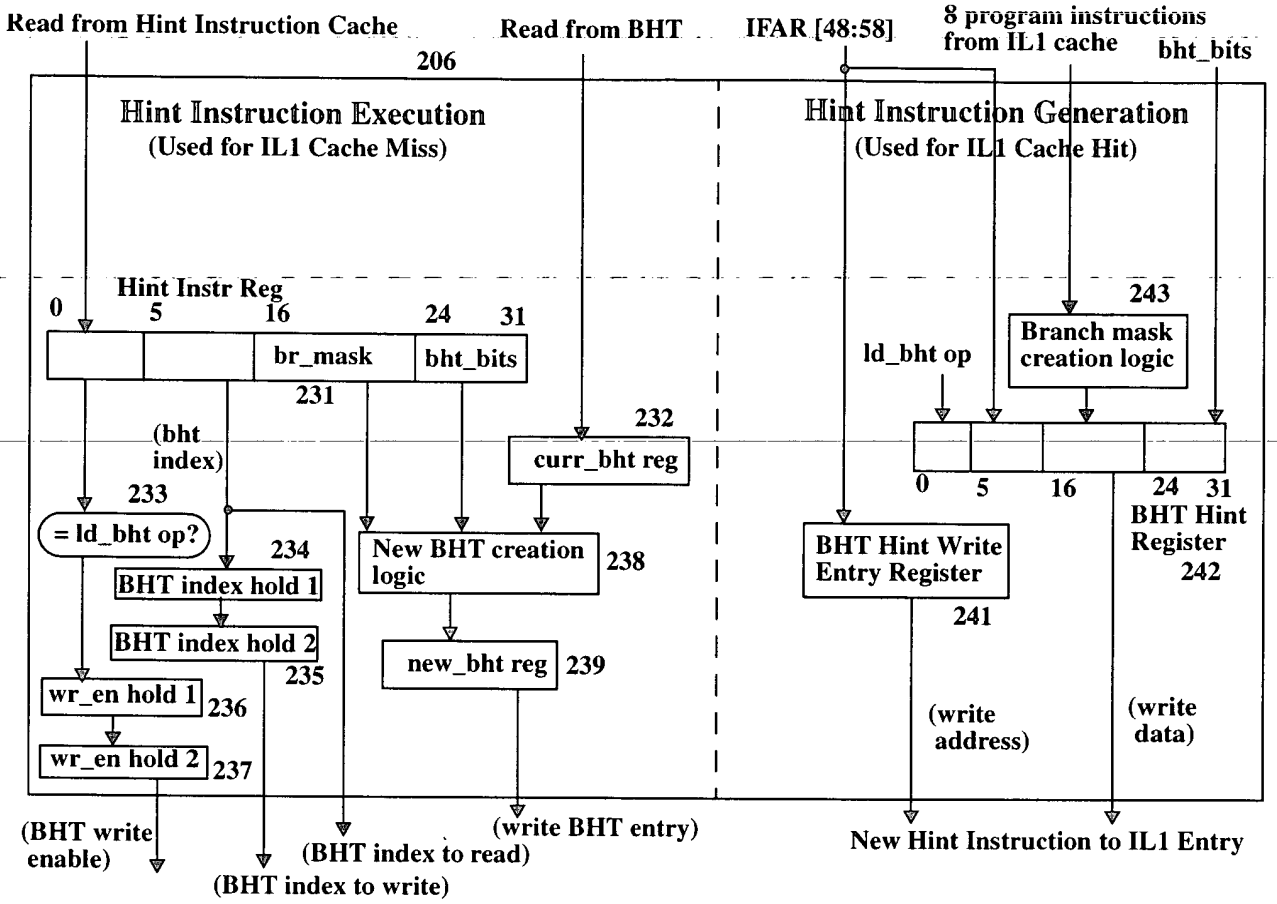


Figure 2B New BHT creation logic 238

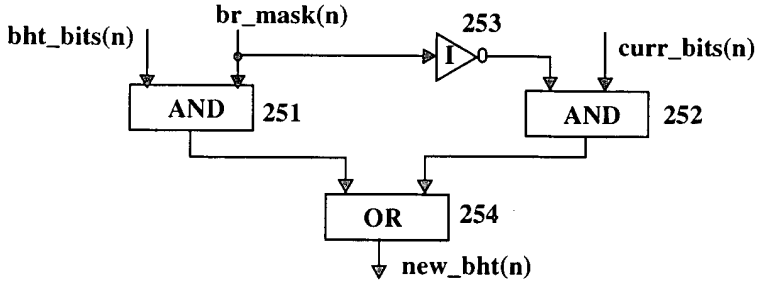


Figure 3

Overview of the Instruction Fetch Unit with Hint Processor

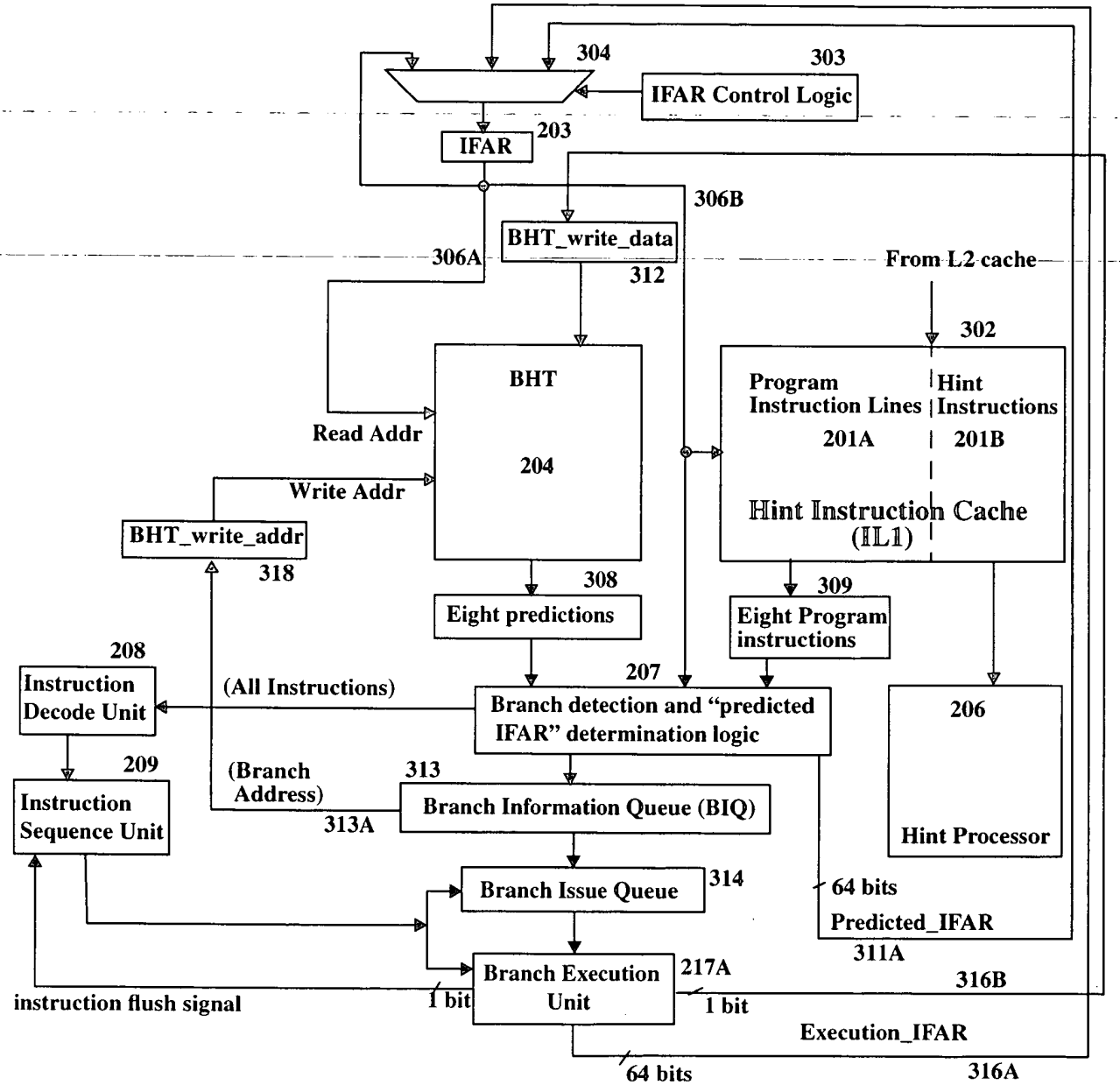
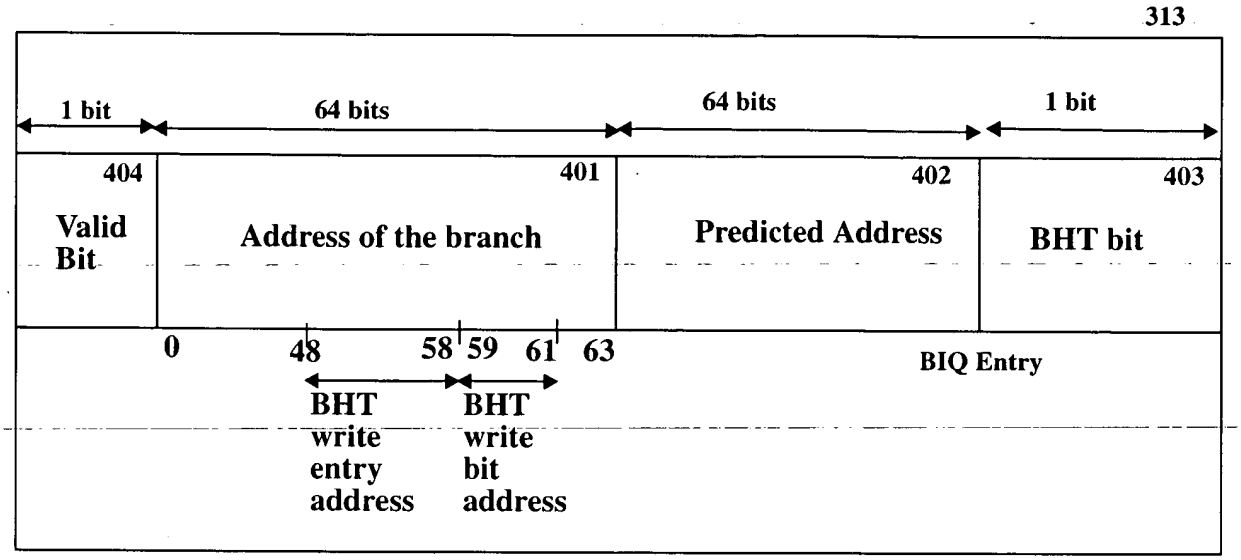
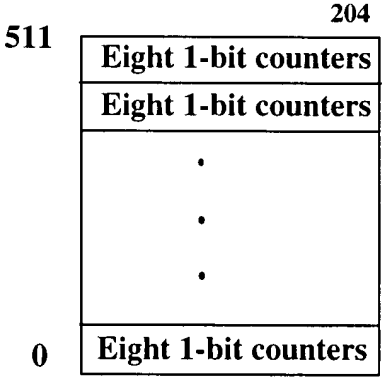


Figure 4



Branch Information Queue (BIQ)

Figure 5



BHT

Figure 6

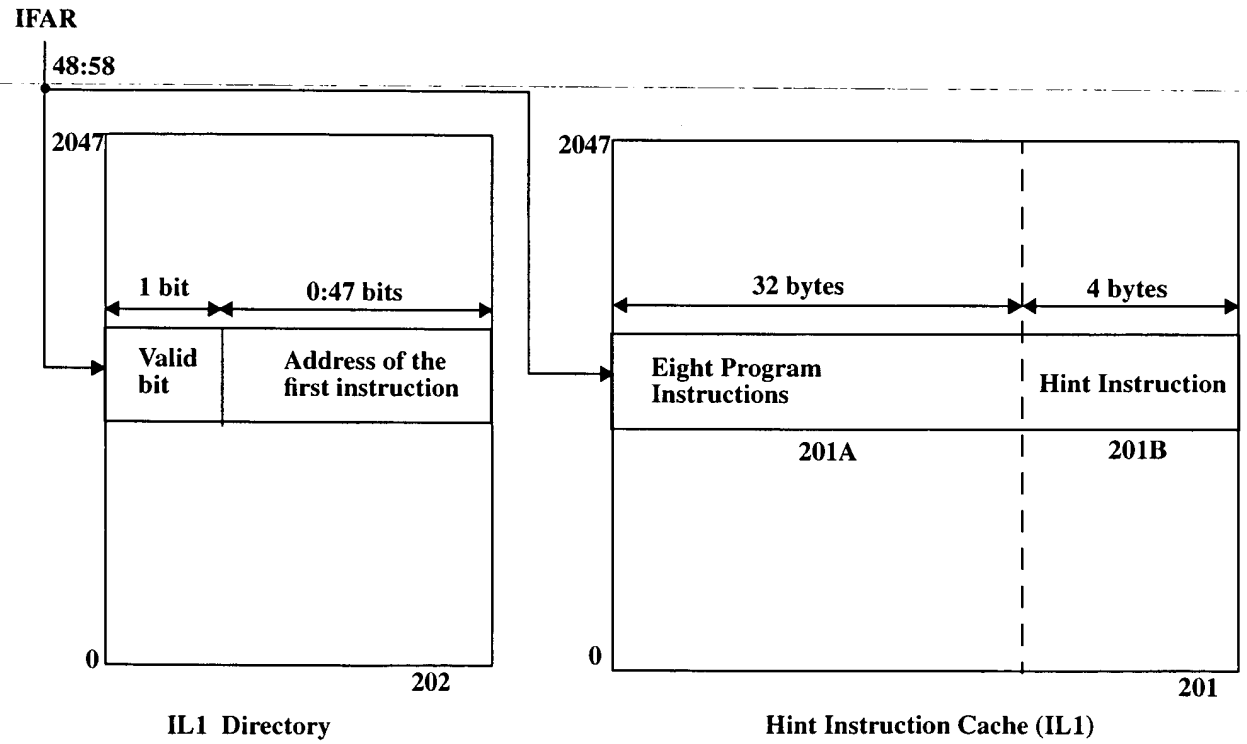

IFAR
48:58
2047
1 bit
0:47 bits
Valid bit
Address of the first instruction
0
202
IL1 Directory
2047
32 bytes
4 bytes
Eight Program Instructions
Hint Instruction
201A
201B
0
201
Hint Instruction Cache (IL1)

Figure 7

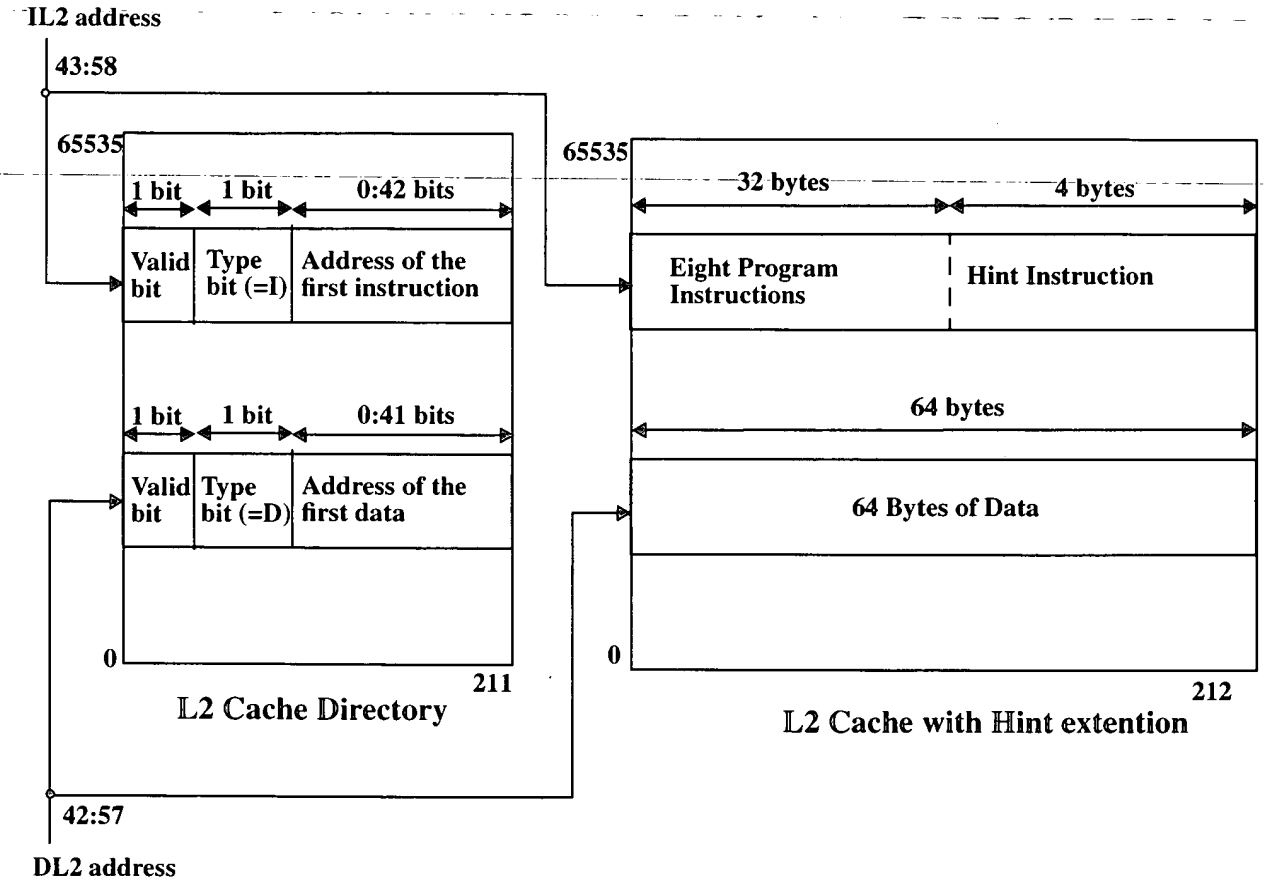

IL2 address
43:58
65535
1 bit
1 bit
0:42 bits
Valid bit
Type bit (=I)
Address of the first instruction
1 bit
1 bit
0:41 bits
Valid bit
Type bit (=D)
Address of the first data
0
211
L2 Cache Directory
65535
32 bytes
4 bytes
Eight Program Instructions
Hint Instruction
64 bytes
64 Bytes of Data
0
212
L2 Cache with Hint extention
42:57
DL2 address

Figure 8

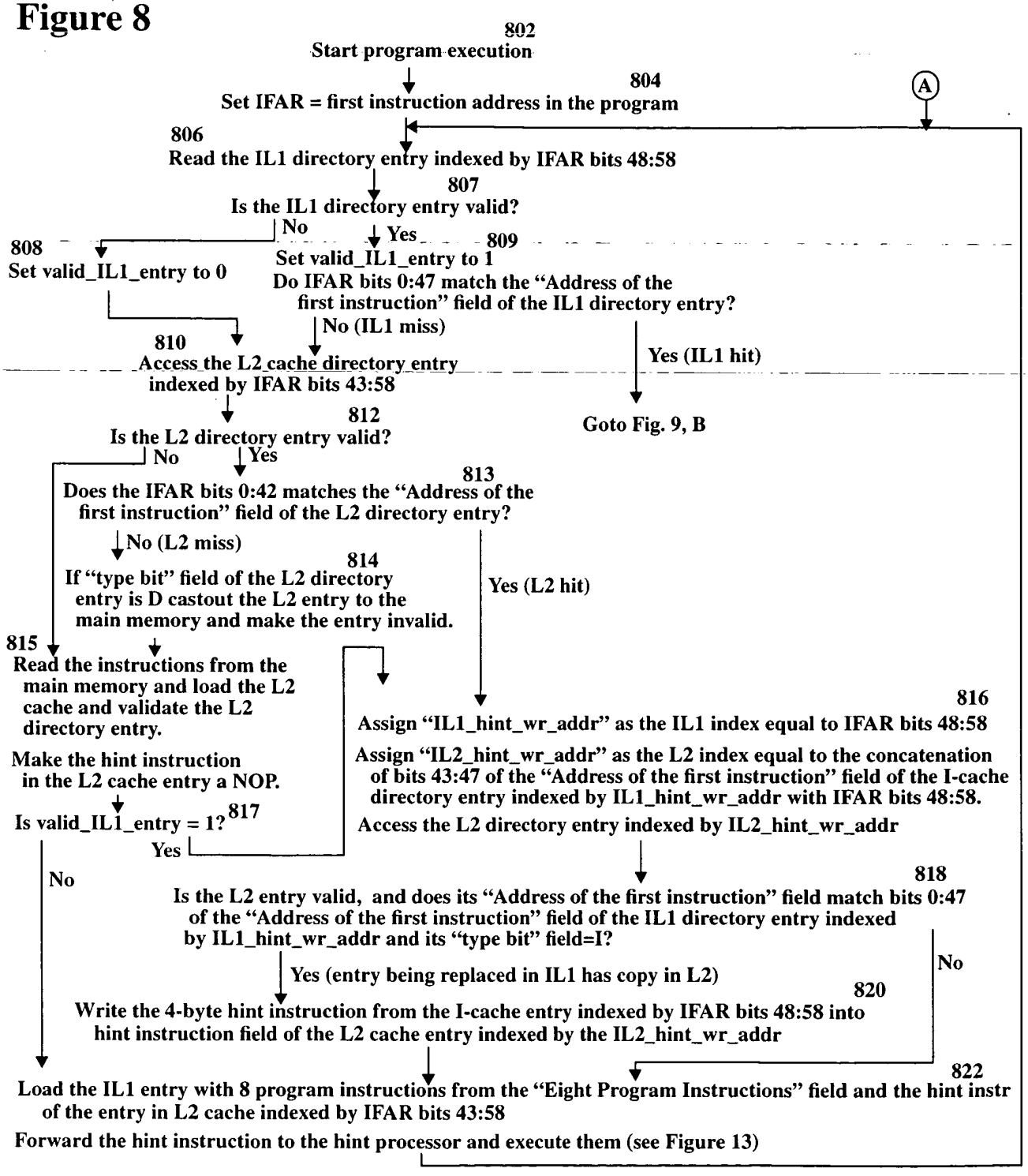

802
Start program execution
804
Set IFAR = first instruction address in the program
A
806
Read the IL1 directory entry indexed by IFAR bits 48:58
807
Is the IL1 directory entry valid?
No
Yes
808
Set valid_IL1_entry to 0
809
Set valid_IL1_entry to 1
Do IFAR bits 0:47 match the "Address of the first instruction" field of the IL1 directory entry?
No (IL1 miss)
Yes (IL1 hit)
Goto Fig. 9, B
810
Access the L2 cache directory entry indexed by IFAR bits 43:58
812
Is the L2 directory entry valid?
No
Yes
813
Does the IFAR bits 0:42 matches the "Address of the first instruction" field of the L2 directory entry?
No (L2 miss)
Yes (L2 hit)
814
If "type bit" field of the L2 directory entry is D castout the L2 entry to the main memory and make the entry invalid.
815
Read the instructions from the main memory and load the L2 cache and validate the L2 directory entry.
Make the hint instruction in the L2 cache entry a NOP.
Is valid_IL1_entry = 1?
817
Yes
No
816
Assign "IL1_hint_wr_addr" as the IL1 index equal to IFAR bits 48:58
Assign "IL2_hint_wr_addr" as the L2 index equal to the concatenation of bits 43:47 of the "Address of the first instruction" field of the I-cache directory entry indexed by IL1_hint_wr_addr with IFAR bits 48:58.
Access the L2 directory entry indexed by IL2_hint_wr_addr
818
Is the L2 entry valid, and does its "Address of the first instruction" field match bits 0:47 of the "Address of the first instruction" field of the IL1 directory entry indexed by IL1_hint_wr_addr and its "type bit" field=I?
Yes (entry being replaced in IL1 has copy in L2)
No
820
Write the 4-byte hint instruction from the I-cache entry indexed by IFAR bits 48:58 into hint instruction field of the L2 cache entry indexed by the IL2_hint_wr_addr
822
Load the IL1 entry with 8 program instructions from the "Eight Program Instructions" field and the hint instr of the entry in L2 cache indexed by IFAR bits 43:58
Forward the hint instruction to the hint processor and execute them (see Figure 13)

Figure 9

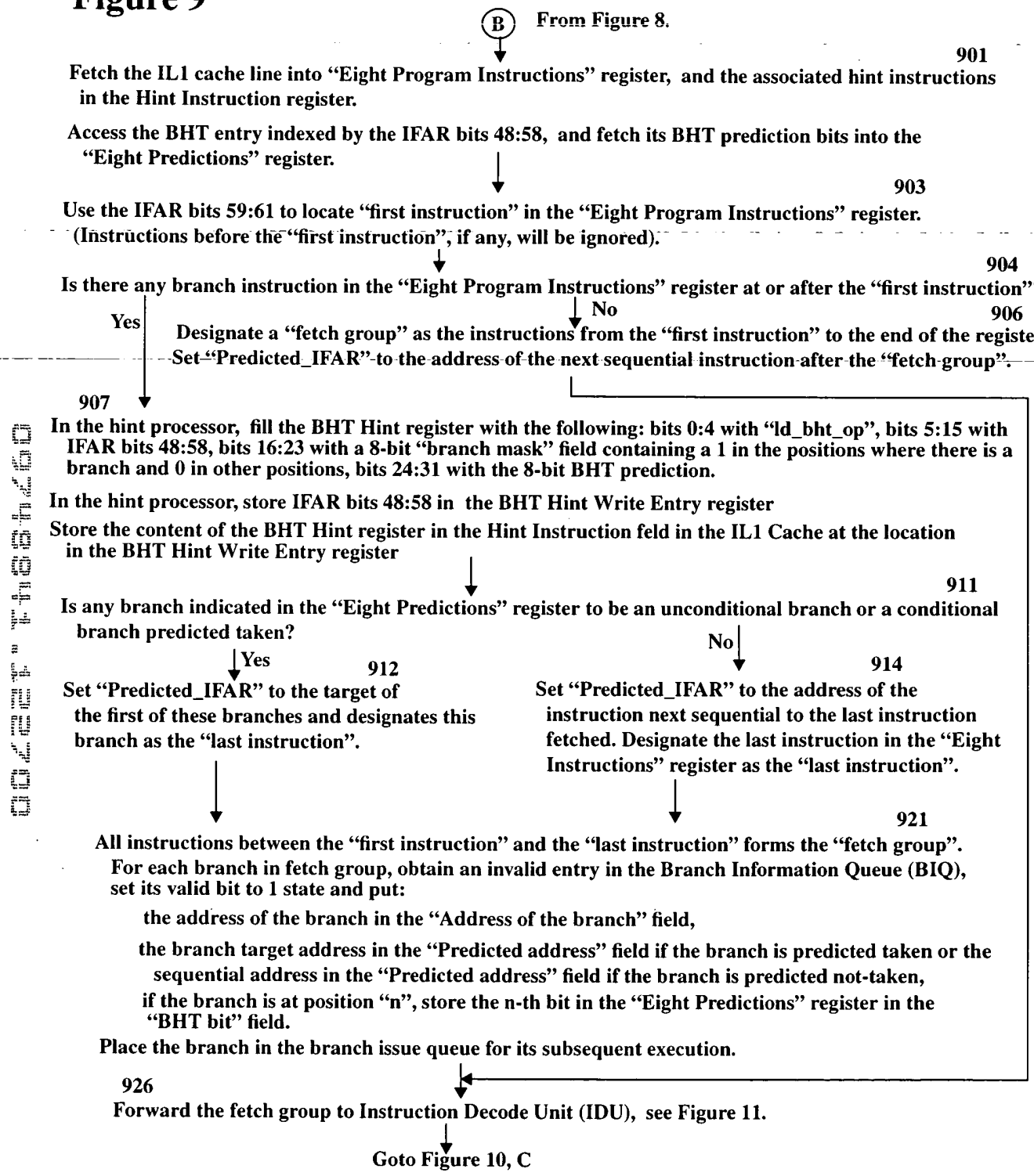

B
From Figure 8.
901
Fetch the IL1 cache line into "Eight Program Instructions" register, and the associated hint instructions in the Hint Instruction register.
Access the BHT entry indexed by the IFAR bits 48:58, and fetch its BHT prediction bits into the "Eight Predictions" register.
903
Use the IFAR bits 59:61 to locate "first instruction" in the "Eight Program Instructions" register. (Instructions before the "first instruction", if any, will be ignored).
904
Is there any branch instruction in the "Eight Program Instructions" register at or after the "first instruction"?
Yes
No
906
Designate a "fetch group" as the instructions from the "first instruction" to the end of the register. Set "Predicted_IFAR" to the address of the next sequential instruction after the "fetch group".
907
In the hint processor, fill the BHT Hint register with the following: bits 0:4 with "ld_bht_op", bits 5:15 with IFAR bits 48:58, bits 16:23 with a 8-bit "branch mask" field containing a 1 in the positions where there is a branch and 0 in other positions, bits 24:31 with the 8-bit BHT prediction.
In the hint processor, store IFAR bits 48:58 in the BHT Hint Write Entry register
Store the content of the BHT Hint register in the Hint Instruction feld in the IL1 Cache at the location in the BHT Hint Write Entry register
911
Is any branch indicated in the "Eight Predictions" register to be an unconditional branch or a conditional branch predicted taken?
Yes
912
Set "Predicted_IFAR" to the target of the first of these branches and designates this branch as the "last instruction".
No
914
Set "Predicted_IFAR" to the address of the instruction next sequential to the last instruction fetched. Designate the last instruction in the "Eight Instructions" register as the "last instruction".
921
All instructions between the "first instruction" and the "last instruction" forms the "fetch group".
For each branch in fetch group, obtain an invalid entry in the Branch Information Queue (BIQ), set its valid bit to 1 state and put:
the address of the branch in the "Address of the branch" field,
the branch target address in the "Predicted address" field if the branch is predicted taken or the sequential address in the "Predicted address" field if the branch is predicted not-taken,
if the branch is at position "n", store the n-th bit in the "Eight Predictions" register in the "BHT bit" field.
Place the branch in the branch issue queue for its subsequent execution.
926
Forward the fetch group to Instruction Decode Unit (IDU), see Figure 11.
Goto Figure 10, C

Figure 10

Next IFAR determination logic

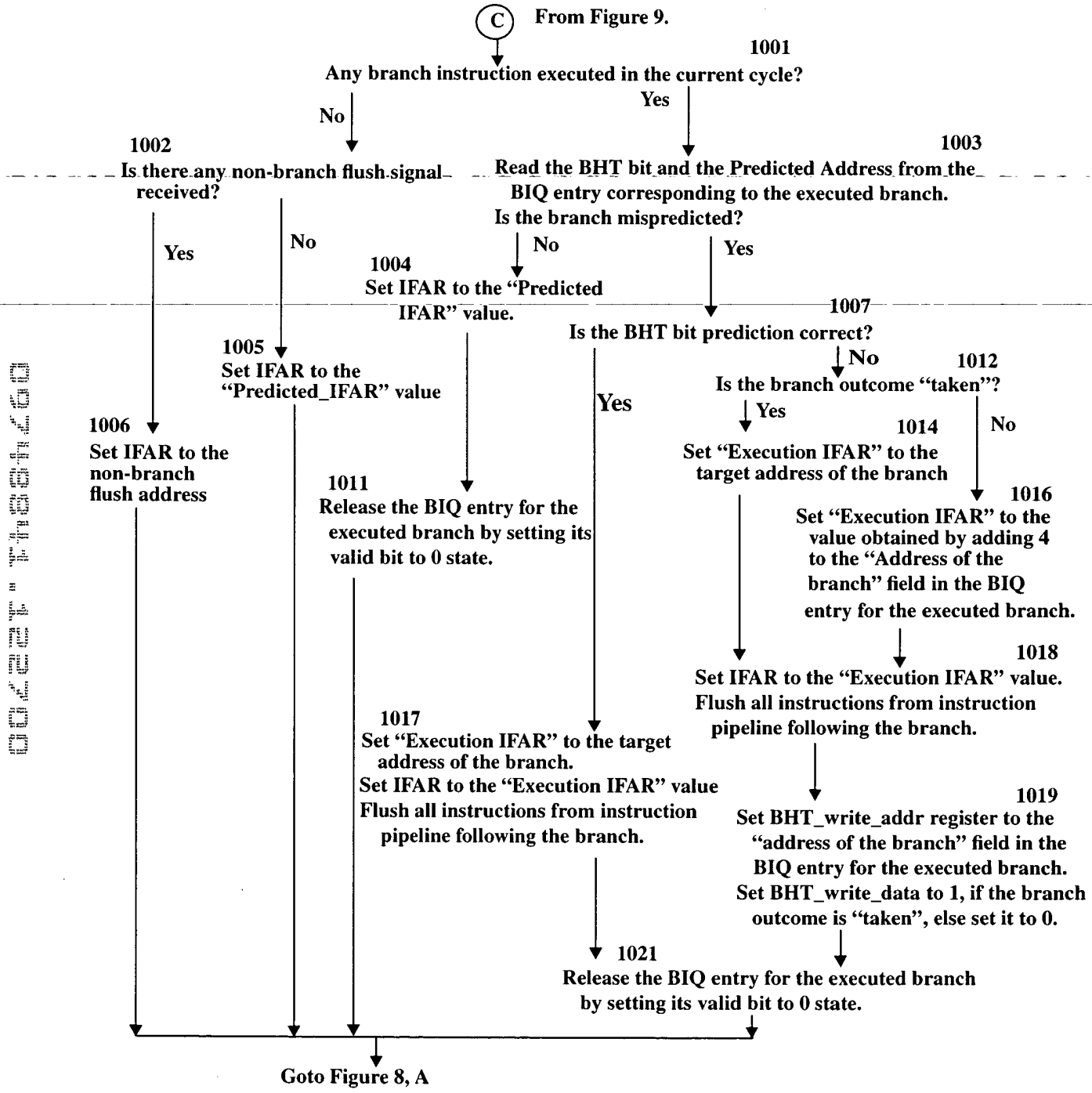


Figure 11

Instruction Decode and Dispatch

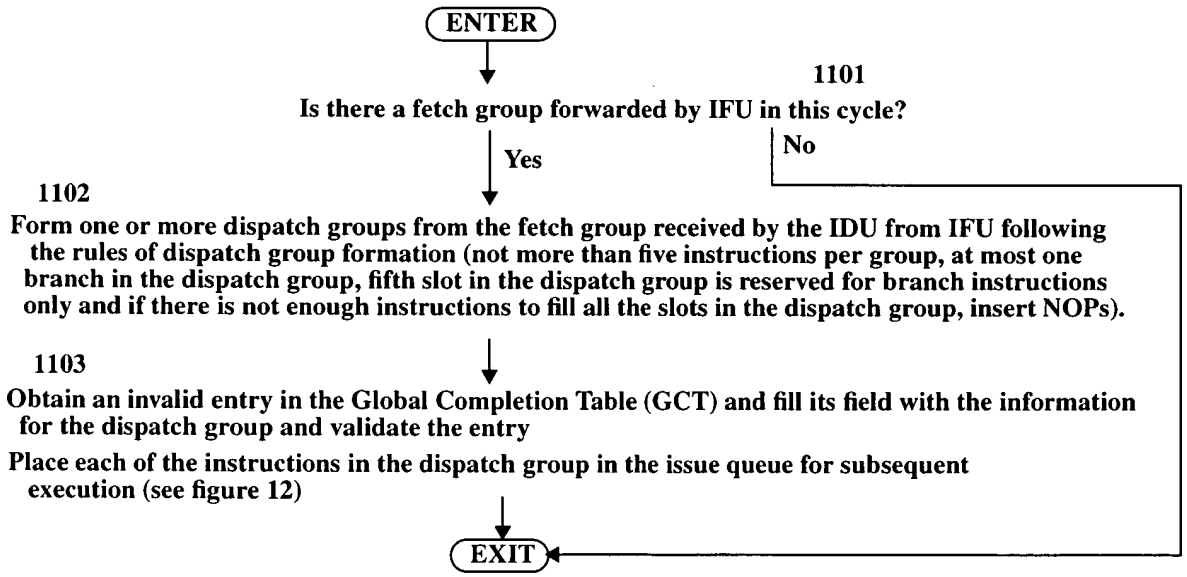


Figure 12

Instruction issue and instruction execution

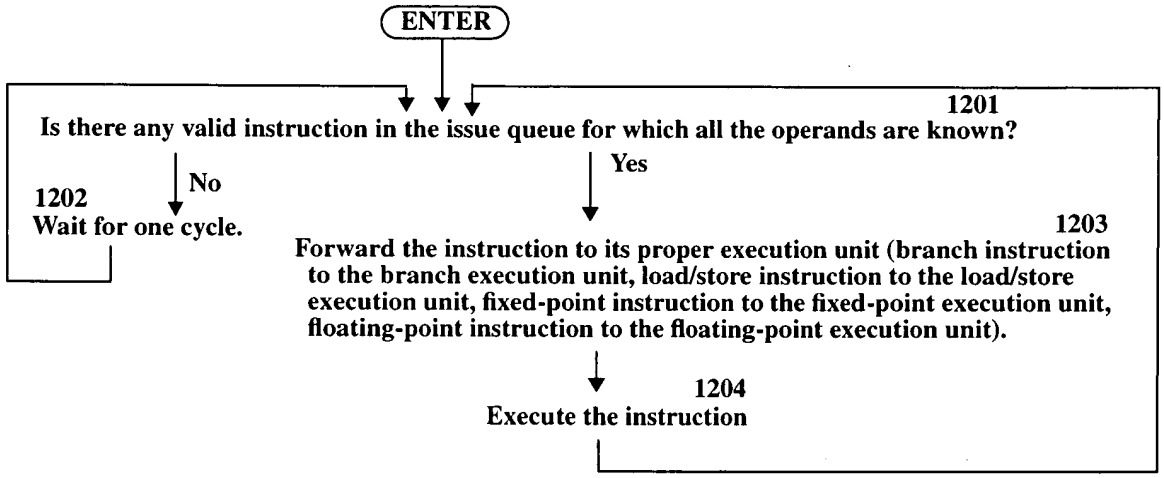


Figure 13

Execution in the Hint Processor for each IFAR cycle